CLAIMS

What is claimed is:

1. A method of forming a programmable logic array (PLA), comprising:

receiving a description of functionality to be implemented by the PLA;

preparing a PLA model that contains only programmable connections necessary to implement the described functionality;

selectively adding programmable connections to the PLA model to allow for programming of other functionality.

2. The method of claim 1, wherein the step of selectively adding programmable connections includes adding programmable connections such that the PLA programmed with the described functionality has certain performance characteristics, and wherein the PLA programmed with other functionality has the same performance characteristics.

3. The method of claim 1, wherein the PLA model has a non-regular physical structure.

4. The method of claim 1, further including:

receiving a minimum performance goal;

after selectively adding programmable connections, testing the PLA model to determine if it meets or exceeds the minimum performance goal;

if the PLA design exceeds the minimum performance goal, selectively adding further programmable connections until the PLA model just meets or only minimally exceeds the minimum performance goal.

5. The method of claim 1, wherein:

the step of receiving includes receiving a plurality of descriptions of functionality, each description to be independently implemented by the PLA;

the step of preparing includes preparing a PLA model where the PLA model contains only the programmable connections necessary to implement the described functionality of the descriptions.

6. The method of claim 1, further including:

evaluating the description to determine if pre-array or post-array logic is useful.

7. The method of claim 1, wherein:

selectively adding programmable connections includes adding programmable connections for shared and spare terms.

8. The method of claim 1, wherein:

selectively adding programmable connections includes adding programmable connections for complementing terms.

9. The method of claim 1, wherein:

selectively adding programmable connections includes adding programmable connections for complementing parts of product terms.

10. The method of claim 1, wherein:

the programmable connections each include a storage device and a logic gate; and

the PLA includes product terms and sum terms formed with gate trees.

11. A method of forming a programmable logic array (PLA), comprising:

receiving a description of functionality to be implemented by the PLA;

preparing a PLA model with a depopulated array;

selectively re-populating the array in the PLA model to allow for programming of other functionality.

12. The method of claim 11, wherein the depopulated array is an AND array.

13. The method of claim 11, wherein the depopulated array is an OR array.

14. The method of claim 11, wherein the array has a non-regular physical structure.

15. A method of forming a programmable logic array (PLA), comprising:

receiving a description of functionality to be implemented by the PLA;

preparing a PLA model sized to accommodate the described functionality and fully populated with programmable connections;

removing from the PLA model all programmable connections not necessary to implement the described functionality;

selectively adding programmable connections to the PLA model; and

building a PLA based on the PLA model.

16. The method of claim 15, wherein the step of selectively adding includes selectively adding programmable connections to the PLA model for shared and spare product terms.

17. The method of claim 15, wherein the step of building includes building a PLA having a non-regular physical structure.

18. A method of forming a programmable logic array (PLA), comprising:

receiving a plurality of descriptions of functionality to be implemented by the PLA;

preparing a PLA model that contains only programmable connections necessary to implement the described functionality of the descriptions; and

selectively adding programmable connections to the PLA model to allow for programming of other functionality.

19. A method of forming a programmable logic array (PLA), comprising:

receiving a plurality of descriptions of functionality to be implemented by the PLA;

preparing a PLA model where the PLA model is sized to accommodate the largest described functionality in the plurality of descriptions;

removing from the PLA model programmable connections not necessary to implement the described functionality of the descriptions.

20. The method of claim 19, further including:

selectively adding programmable connections to the PLA model to allow for programming of other functionality.

21. A method of forming a programmable logic array (PLA), comprising:

receiving a description of functionality to be implemented by the PLA;

determining if pre-array or post-array logic will be useful to enhance the speed or reduce the size of the PLA;

preparing a PLA model based upon the step of determining.

22. The method of claim 21, wherein the step of preparing further includes:

preparing a PLA model with at least a partially depopulated array.

23. The method of claim 21, further including building the PLA based on the PLA model.

24. An integrated circuit, comprising:

a programmable logic array (PLA) having a non-regular structure.

25. The integrated circuit of claim 24, wherein:

the PLA has been depopulated to include only programmable connections necessary to implement certain functionality to be implemented by the PLA.

26. The integrated circuit of claim 24, wherein the PLA includes:

programmable connections necessary to implement certain known functionality to be implemented by the PLA; and

programmable connections strategically selected to accommodate future programming of other functionality, but that do not amount to full population of programmable connections.

27. The integrated circuit of claim 24, wherein the PLA includes:

programmable connections that include a storage device and a logic gate; and

product terms and sum terms formed with gate trees.

28. The integrated circuit of claim 24, wherein the PLA includes

programmable connections that include:

a pair of storage devices; and

a multiplexer.

29. The integrated circuit of claim 24, wherein the PLA includes:

an AND array that includes programmable connections that each include a pair of storage devices and a multiplexer; and

an OR array that includes programmable connections that each include only one storage device and a logic gate.

30. The integrated circuit of claim 24, wherein the PLA is constructed so that it maintains its performance characteristics on reprogramming.

31. An integrated circuit, comprising:

a programmable logic array (PLA) depopulated to include programmable connections only where required to implement certain known functionality and selectively minimally repopulated to accommodate future programming of other functionality.

32. The integrated circuit of claim 31, wherein:

the PLA programmed with the known functionality has certain performance characteristics, and wherein the PLA programmed with other functionality has the same performance characteristics.

33. The integrated circuit of claim 31, wherein:

the programmable connections include a storage device and a logic gate;

the PLA includes product terms and sum terms formed with gate trees.

34. The integrated circuit of claim 33, wherein:

the storage device is one of a latch or a flip-flop; and

the logic gate is an OR gate.

35. The integrated circuit of claim 33, wherein:

the storage device is one of a latch or a flip-flop; and

the logic gate is a multiplexer.

36. The integrated circuit of claim 31, wherein:

the programmable connections include a pair of storage devices and a multiplexer.

37. The integrated circuit of claim 31, wherein the PLA includes:

an AND array with a first type of programmable connection; and

an OR array with a second type of programmable connection.

38. The integrated circuit of claim 31, wherein the PLA includes:

an AND array with programmable connections that each include a pair of storage devices and a multiplexer; and

an OR array with programmable connections that each include only one storage device and a logic gate.

39. The integrated circuit of claim 31, wherein the PLA includes:

programmable connections for shared terms, spare terms, and complemented terms.

40. An integrated circuit, comprising:

a programmable logic array (PLA) having a depopulated array that includes programmable connections only where required to implement certain known functionality and selectively minimally repopulated to accommodate future programming of other functionality.

41. The integrated circuit of claim 40, wherein the depopulated array is an AND array.

42. The integrated circuit of claim 40, wherein the depopulated array is an OR array.

43. A programmable logic array, including:

programmable connections that include a storage device and a logic gate; and

product terms that include a gate tree.

44. The programmable logic array of claim 43, wherein:
the storage device is one of a latch or a flip-flop;
the logic gate is one of a multiplexer or an OR gate.

45. A programmable logic array, including:
programmable connections that include a pair of storage devices and a multiplexer.

46. The programmable logic array of claim 45, further including:
product terms formed with AND trees; and
sum terms formed with OR trees.

47. A programmable logic array (PLA), including:
an AND array that includes a first type of programmable connection; and
an OR array that includes a second type of programmable connection.

48. The PLA of claim 47, wherein:
the first type of programmable connection includes a pair of storage devices and a multiplexer;
the second type of programmable connection includes only one storage device and a logic gate.

49. A computer readable storage medium having instructions stored therein to be used in forming a programmable logic array (PLA), which instructions when executed by a computer cause the computer to perform the steps of:
receiving a description of functionality to be implemented by the PLA;
preparing a PLA model that contains only programmable connections necessary to implement the described functionality;
selectively adding programmable connections to the PLA model to allow for programming of other functionality.

50. A computer readable storage medium having instructions stored therein to be used in forming a programmable logic array (PLA), which instructions when executed by a computer cause the computer to perform the steps of:

receiving a description of functionality to be implemented by the PLA;

preparing a PLA model with a depopulated array;

selectively re-populating the array in the PLA model to allow for programming of other functionality.